Hardware Implementation of Increasing Efficiency for Golay Code

Shmalin Niranjana. S, Subalakshmi. G, Subashini. R, Surya. T
Dept. of ECE, M.Kumarasamy College of Engineering, Karur

Abstract: This paper explains about the cyclic redundancy check-based encoding scheme and implements the encoding algorithm efficiently in FPGA based model for each the binary Golay code (G23) and extended binary Golay code (G24). In Virtex-4 FPGA, low latency of high speed design has been designed for Golay encoder without using linear feedback shift register. Based on an incomplete maximum likelihood decoding scheme, low complexity decoding architecture is presented for extended binary Golay code(24, 12, 8). The decoder architecture which is proposed in this paper has very low latency and occupies less area than the other architectures. The clock frequency for decoder is 195.028 and the encoder module operates at 238.575. Error correction can be done using the implemented hardware which is used in high speed applications like communication link.

I.INTRODUCTION

The digital coding is used to correct errors in a system with the help of Golay code. There are two types of Golay code: binary Golay code (G23) which is known as (23, 12, 7) and extended binary Golay code (G24) which is known as (24, 12, 8). The Weighted eradication codec has been utilized broadly in profound space system of JPL-NASA and in addition in the Voyager imaging framework with the assistance of extended golay code. Golay code utilized as a part of various applications like coded excitation for a laser and ultrasound imaging because of the entire side lobe invalidation property of integral Golay pair. However, a high cost unique design pattern generator is utilized for creating Golay code. In error correction, rapid and high throughput equipment for decoder is utilized in communication process.

Several papers have contributed to the encoding methods of golay code. These papers have complex algorithms and hence implementing hardware is not appropriate. Weighted erasure codec for the extended Golay code is proposed. It consists of a parity generator, a clock doubler, LFSR, switching logics and a 5 bit counter. Generally, designing of hardware uses CRC generation. Here, the throughput is very less and the inactivity is high, henceforth making it not reasonable for rapid applications. Decoding architecture is based on IMLD scheme.

In Binary Golay code (23, 12, 7), 23 bits is the length of the codeword, 12 is the message bit and 7 bits is the minimum distance between the codes. B. Arithmetic operations are done using GF with the help of generator polynomial. In golay code, the polynomials are generally represented as $x11 + x10 + x6 + x5 + x4 + x2 + x1$ and $x11 + x9 + x7 + x6 + x5 + x1 + 1$. Usually, the extended Golay code is generated by appending one parity bit. Check bits is produced after the long division The matrix B is given as,

$$B=\begin{bmatrix} 1&1&0&1&1&1&0&0&0&1&0&1 \\ 1&0&1&1&1&0&0&0&1&0&1&1 \\ 0&1&1&1&0&0&0&1&0&1&1&1 \\ 1&1&1&0&0&0&1&0&1&1&0&1 \\ 1&1&0&0&0&1&0&1&1&0&1&1 \\ 1&0&0&0&1&0&1&1&0&1&1&1 \\ 0&0&0&1&0&1&1&0&1&1&1&1 \\ 0&0&1&0&1&1&0&1&1&1&0&1 \\ 0&1&0&1&1&0&1&1&1&0&0&1 \\ 1&0&1&1&0&1&1&1&0&0&0&1 \\ 0&1&1&0&1&1&1&0&0&0&1&1 \\ 1&1&1&1&1&1&1&1&1&1&1&0 \end{bmatrix}$$

III. PROPOSED ARCHITECTURE AND ALGORITHM WITH COMPARED RESULTS FOR ENCODER

A. Calculation for Encoder

The means to fulfill the encoding strategy are enrolled as takes after.

1) A characteristic polynomial G(x) is decided for check bits generation.
2) 11 zeros are annexed to one side of message M(x), to such an extent that resultant polynomial P(x) takes in long division handle with G(x).

3) The rest of with the exception of the most noteworthy piece came about toward the finish of the division operation are the check bits for G23. The appending check bits with the message gives us the encoded Golay codeword.
4) An equality bit is added to change over binary Golay code into developed extended Golay code. On the off chance that the heaviness of two binary Golay code is even, then equality bit 0 is annexed, generally 1 is annexed.

The proposed encoder algorithm follows the basic CRC generation process and includes a method for converting binary Golay code to extended Golay code before proceeding for designing architecture.

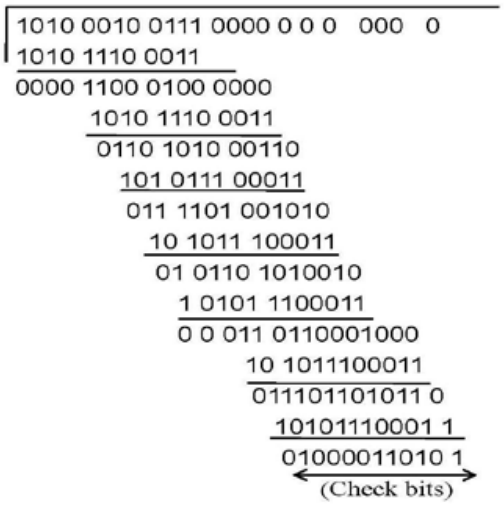

Fig 1. Check bits generation.

The proposed encoder calculation takes after the fundamental CRC bits prepare and incorporates a technique for changing over binary Golay code to extended Golay code before continuing for outlining design. The message to be encoded is A27h. Thus, M(x) = A27h and P(x) in two binary arrangement is spoken to as 1010 0010 0111 0000 000. At long last, the produced check bits in hexadecimal organization are 435h. Thus, the encoded codeword for the message bits (A27h) is A27435h. It brings about binary Golay code word. To change over it into a developed Golay code, an equality bit 1 is included. At long last, the created Golay (24, 12, 8) codeword is (1010 0010 0111 10000110 101 1). By measuring the heaviness of the code, the credibility of the produced Golay code can be tried. The heaviness of each G24 code ought to be a various of four and more noteworthy than equivalent to eight. The created code word illustration has a weight of 12, which is a different of four and more noteworthy than eight. Thus, legitimate code is produced.

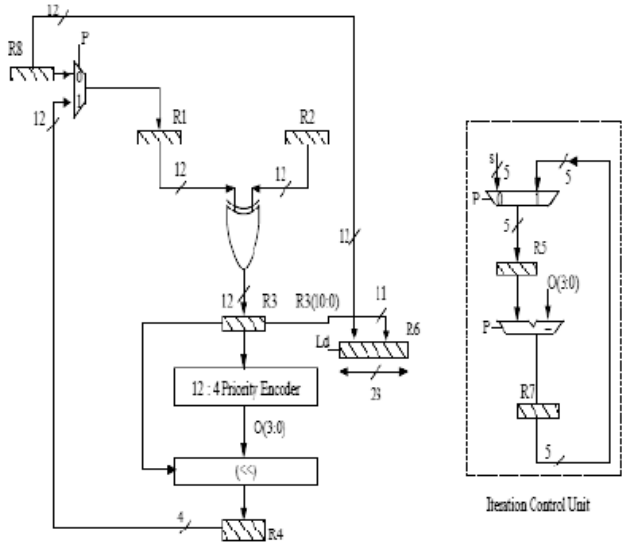

Fig 2. Binary Golay code generation

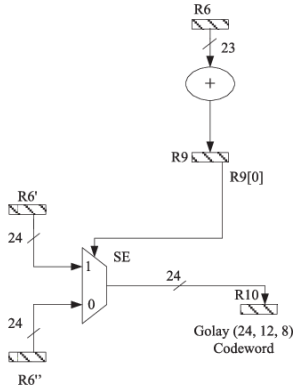

Fig 3. Converting binary Golay code to extended Golay code.

B. Design for Binary Golay Code and Extended Golay Code

The whole design is separated into two sections, one is to create G23 and the other is utilized for the transformation of G23 to G24. During polynomial division, for modulo-2 subtraction two binary XOR operation happens. At every progression during the division procedure, remaining outcome got which is circularly left moved by number of driving zeros present in the outcome. To identify the quantity of driving zeros before initial one piece in the residual result a 12:4 need encoder is utilized. To move the middle of the road result by the yield of need encoder a round move register is utilized. Keeping in mind the end goal to choose the underlying message or the circularly moved middle of the road result a 2:1 multiplexer is utilized. For the multiplexer the control signal is utilized and p is for signifying the controlled subtractor, which is bit wise OR operation of need encoder yield.

The Loop control system is utilized as a part of controlled subtractor. In the subtractor, one information is relegated with 11. Multiplexer is chosen after every cycle and subsequently the quantity of zeros is overhauled in the register R7. The second contribution of the subtractor is the yield of the need encoder. The aftereffect of the subtractor is zero after the last procedure. The last yield is put away in register R7. At the point when the substance in the register R7 gets to be distinctly zero, R6 register is stacked. This demonstrates the finish of both the division procedure and furthermore the check bits handle. The stacking of substance in the enroll of the R3 [10:0] is controlled by the control signal Ld.

Transformation of binary Golay code to extended Golay code is actualized by method for Hardware design. Register R9 stores the heaviness of the two binary Golay code. Substance of R6 included with 0 and R6'' stores the substance of R6 included with 1.Depending upon the zeroth position in the enroll R6, the 2:1 multiplexer chooses either R6'or R6'',which goes about as the select line for the multiplexer. In the outcome, R10 contains Golay (24, 12, 8) encoded codeword.

TABLE I
COMPARISON OF PROPOSED ENCODER ARCHITECTURE CONSIDERING LATENCY AND CLOCKING MECHANISM

Attribute	[5]	Proposed
Latency(Clock Cycles)	23	12(Maximum)
Clocking Mechanism	System Clock + Clock Doubler	System Clock

TABLE II
COMPARISON OF PROPOSED ENCODER ARCHITECTURE BY CONSIDERING LATENCY AND LUT UTILIZATION

Reference	LUT Utilization (%)	Latency(Clock Cycles)
[7]	1.33	12
[8]	1.72	12
Proposed	0.14	12

C. Results of Hardware Implemented Encoder Module

MATLAB R2009b tool is used to verify the proposed algorithm for encoder and the module is simulated using Xilinx ISE tool and implemented in XC4vlx160-12 ff1148 FPGA. The encoder module has the working recurrence 238.575MHz. To make a high information rate empowered framework, codeword per clock cycle is utilized rather than single check bit per check cycle in the proposed engineering. 187 look into tables are utilized as a part of this engineering. The aggregate cell territory is 12389.83 μm2 and the aggregate power utilized by design is 963.52 μW.

To decrease power and zone additional checking component is maintained a strategic distance from in the proposed design which is spoken to in the table I. The inactivity is lessened in the proposed design where the most extreme of 12 clock cycles is utilized.

It clarifies that the proposed architecture beats parallel CRC-11 circuits as far as rate of LUT usage where same inactivity. The parallel execution utilizes critical increment in region (5%–10% for each piece). Henceforth, it is avoided.

IV. PROPOSED ARCHITECTURE AND ALGORITHM WITH COMPARED RESULTS FOR DECODER

A. Calculation for Decoding Extended Golay Code

IMLD calculation utilizes Algorithm 1 are for decoding the augmented binary Golay code. Here the codeword is gotten as W, ith line of network B as bi and error design as u. Two disorders (S and SB) are conceivable because of plausibility of two equality check grids (either [I|B] or [B|I]).

B. Proposed Architecture for Decoding Extended Golay Code

1) Weight Measurement Unit:

For including the quantity of 1s the arrangement, weight estimation unit is required. The circuit utilized for this estimation unit brings about less basic way delay.

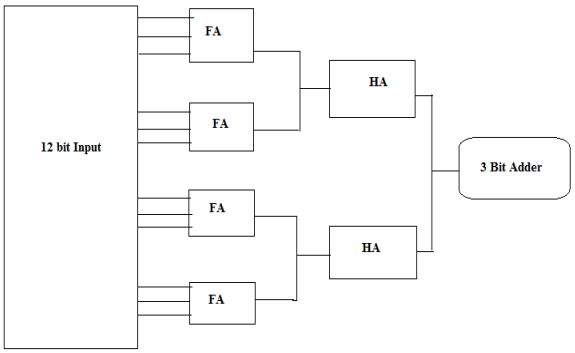

Fig 4. Structure of weight measurement

2) Selection of H+xi and HX+xi for Which Weight Is Less Than Two:

This unit chooses the H+xi or HX+xi for which weight is not as much as equivalent to two. Subsequent to performing for all the 12 registers, the outcome has 12 bits yield. At that point these bits are encouraged to a 12:1 need encoder as data sources. A 13:1 multiplexer is utilized to choose the fancied enroll content, which has fulfilled the weight limitation. The select signal for the multiplexer is the four yield of the need encoder.

C. Consequences of Hardware Implementation of Decoder Module

MATLAB R2009b tool is used to verify the proposed algorithm for encoder and the module is simulated using Xilinx ISE tool and implemented in XC4vlx160-12 ff1148 FPGA. The decoder module has the working recurrence 195.082 MHz To make a high information rate empowered framework, codeword per clock cycle is utilized rather than single check bit per check cycle in the proposed design. 785 look into tables are utilized as a part of this engineering. The aggregate cell zone is 30129.32μm2 and the aggregate power utilized by the design is 14.65 mW.

This decoder design has prefbitsble asset use and speed over alternate works utilizing same calculation for decoder. In the proposed design, inertness of 27 clock cycles is gotten and possesses a zone of 3013 proportional doors. This is the slightest among the various litbitsry works. The proposed design will yield a yield (24 bits) per clock cycle. Accordingly, the proposed architecture for decoder searches useful for high information rate framework.

V. CONCLUSION

Subsequent to checking the proposed calculation, equipment engineering for both paired Golay encoder and expanded double Golay encoder have been planned and actualized productively. This paper beats the burden of traditional LFSR-based CRC bits plans and another equipment design for encoder and decoder is proposed. The equipment modules for encoder and decoder are utilized as a part of utilizations, for example, fast correspondence joins, photograph spectroscopy, and ultrasonography.

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