DESIGN OF ABSOLUTE POSITION ENCODER

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ABSTRACT

The target of the plan is supreme position encoder can be associated with the Input and yield signals which considers an immediate interface to the host processor and to run the relating encoder's lord convention. It is additionally associated with the 10-stick header or subD-15 connector through this encoder. This outline permits the host processor to actuate either the 4-wire RS-485 physical interface to associate with an EnDat 2.2, BiSS, or SSI encoder, or the 2-wire RS-485 interface with control over RS-485 to associate with a HIPERFACE DSL encoder. This encoder is supporting the most widely recognized modern serial interfaces. A flat out rotating encoder decides its position utilizing a static reference point, an outright rotational encoder is naturally ready to convey higher quality criticism like Higher general determination and introduction, Better start up execution as a result of low homing time, Accurate movement discovery along different tomahawks, Multiple yield conventions for better hardware coordination, Better recuperation from framework or power disappointments. Deciding multi-hub introduction for CNC machines utilized as a part of parts assembling, consequently

deciding the tallness of scissor beds utilized as a part of healing centers, Accurately situating various stabilizers for expansive vehicles like cranes or aeronautical lifts, Moving programmed entryways or sounds without a constraining switch and Continuing mechanical development neatly even after a power disappointment. A servo engine is one of the generally utilized variable speed drives in modern generation and process mechanization and building innovation around the world. Which require high exactness situating, speedy turning around and excellent execution. Squirrel confine enlistment engine is utilized for all steady speed applications due to its minimal effort, rough outline and straightforward control outfit. Mechanical computerization is the utilization of control frameworks, for example, PCs or robots, and data advances for dealing with various procedures and hardware in an industry to supplant a person.

INTRODUCTION

Supreme position encoders like EnDat 2.2, BiSS, SSI or HIPERFACE DSL. A connector with 3.3V rationale I/O signals takes into consideration guide interface to the host processor like Sitara AM437x or Delfino F28379 run the comparing expert convention. Ace executions are accessible

on Sitara AM437x (EnDat2.2, BiSS AND HIPERFACE DSL) or Delfino Design Drive (EnDat2.2 and BiSS). The TI configuration permits the host processor to choose between a 4-wire encoder interface like EnDat 2.2 and BiSS or a 2-wire interface with control over RS485 like HIPERFACE DSL. To meet the chose encoder's supply extend, the plan offers a programmable yield voltage with either 5.25V or 11V. This current outline's energy supply offers security against over-voltage and short out as per the chose encoder's voltage range to forestall harm amid a link short. TIDA-00179 has been tried up to 100m link length with EnDat 2.2 and 2-wire HIPERFACE DSL encoder. The outline is controlled through industry standard 24V and components a wide info voltage go from15 to 60V. A connector with 3.3V rationale I/O signals takes into consideration an immediate interface to the host processor like SitaraAM437x or C2000MCU to run the comparing encoder's lord convention. The outline permits the host processor to enact either the 4-wireRS-485 physical interface to associate with an EnDat2.2, BiSS, or SSI encoder, or the 2-wire RS-485 interface with control over RS485 to interface with a HIPERFACE DSL encoder. The secured encoder control supply includes a programmable yield voltage of either 5.25 or 11V. The voltage alongside the voltage swell and yield current was guaranteed it is agreeable to the over all supply particular for the encoder benchmarks EnDat2.2, BiSS, SSI, and HIPERFACE DSL. The total position encoder can be associated with the reference plan either through a subD-15 connector or a10-pinheader.The connector has committed pins for interfacing a 2-wire HIPERFACE DSL encoder, which incorporates control over RS-485 and shared pins for EnDat2.2, BiSS, and SSI position encoders. This outline underpins link length so fup to no less than 100m.

BLOCK DIAGRAM
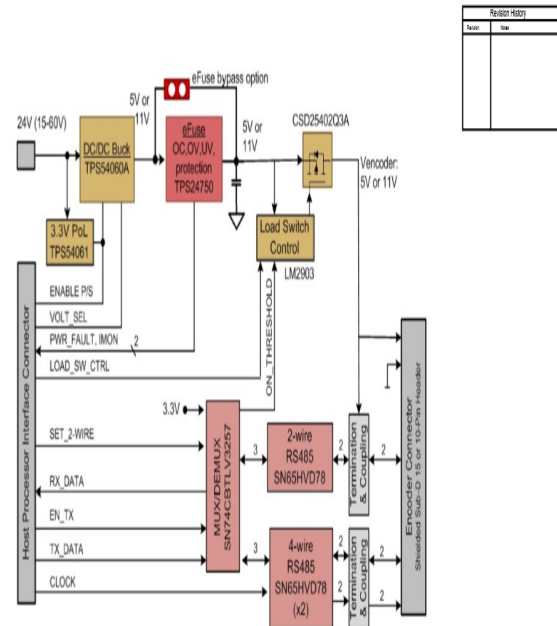
EnDat 2.2

The EnDat 2.2 interfaces from HEIDENHAIN are an absolutely advanced, bidirectional serial interface standard for straight or revolving position input encoders. The EnDat 2.2 ace sends the kind of information transmitted, similar to outright position, parameters, and diagnostics, through mode summons to the encoder. The correspondence just requires four flag wires. Two wires are for the bidirectional differential information (DATA+ and DATA−) and are transmitted into equal parts duplex mode. The other two wires are for the differential clock flag (CLOCK+ and CLOCK−). From the rest of the wires, two wires are utilized for the encoder control supply. The other two wires are utilized for battery buffering or for parallel power supply lines to diminish the link's misfortunes.
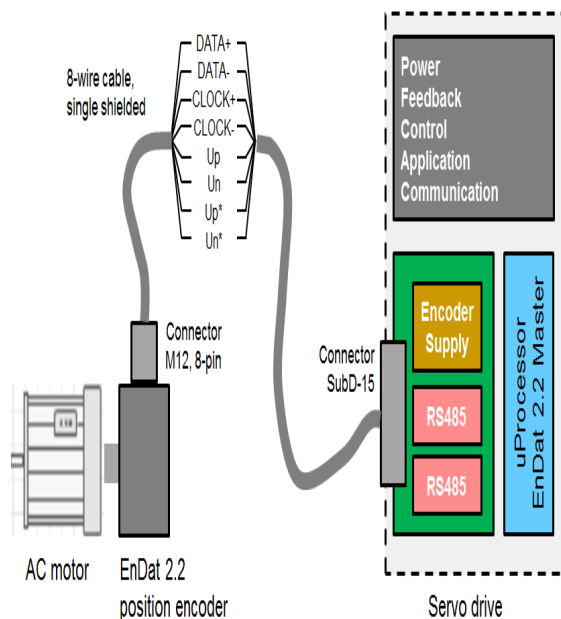
PHYSICAL LAYER

EnDat 2.2 indicates a differential line transmitter and collector as per EIA standard RS-485 for the differential signs CLOCK+, CLOCK−, DATA+, and DATA−. The differential DATA+ and DATA− signs are bidirectional half-duplex, and the RS-485 handset is designed in directional mode with DE and/RE tight together. The differential CLOCK+ and CLOCK− signs are unidirectional and are a yield of the resulting gadgets. The information is transmitted and gotten synchronous to the clock flag, which is produced by the EnDat 2.2 ace. On the EnDat 2.2 ace, the transmit information changes on the falling edge clock edge. Immediately remuneration on the ace, the get information is hooked on the rising clock edge. The clock stays high when there is neither information transmitted nor information got. The clock recurrence is variable. The greatest clock recurrence relies on upon the link length.

BiSS INTERFACE

The BiSS interface is an open source convention presented by iC-Haus GmbH.

BiSS characterizes an advanced bidirectional serial interface for actuators and sensors, for example, rotating or position encoders. BiSS subtle elements can be found at BiSS Interface. BiSS permits serial-synchronous information correspondence in unidirectional mode or bidirectional mode (BiSS-C persistent mode). The BiSS interface is equipment good to the SSI. The BiSS convention characterizes every supporter into the accompanying information segments: sensor information, actuator information, and enroll information. Each area can have different setups as per get to and transmission execution, contingent upon the distinctive sensor application. This convention is alluded to as the BiSS ace that sends and gets information from the position encoder. With BiSS direct or revolving position encoders.

Elements OF BiSS

• 2 unidirectional lines Clock and Data

• Unidirectional

• Bidirectional

HIPERFACE DSL

HIPERFACE DSL is an advanced convention determined and possessed by Sick. HIPERFACE DSL is gotten from HIgh PERformance InterFACE Digital Servo Link. The heartiness of the convention empowers the association with the engine input framework through the engine

association link and improves the establishment of an encoder framework in the drive. Key elements of HIPERFACE DSL 2-wire physical interface are:

• Digital interface consistent to RS-485 standard with an exchange rate of 9.375 MBaud
• Half-duplex correspondence with the encoder through double wires
• Power supply and correspondence with the encoder did utilizing the same double wires. The association links to the encoder are steered as a protected, wound combine link in the power supply link to the engine. Accordingly, no different link for the encoder plug connector is required
• Cable length between the recurrence inverter and the encoder up to 100m without debasement of the working execution HIPERFACE DSL can be utilized as a part of two diverse interface circuit setups. Every design requires an alternate sort of association link. When utilizing a different encoder link, the 4-wire interface is utilized. To utilize a 2-wire link incorporated in the engine link (as appeared in Figure 6), a transformer is required to build normal mode dismissal proportion. The supply voltage and GND are coupled onto the RS-485 differential flags through inductors L1 and L2, and DC is decoupled to the transformer through capacitors C3 and C4, individually.

SSI

SSI is a unidirectional serial convention over RS-422. The unidirectional clock is created by the ace and is indicated from 80 kHz to 2 MHz. The get information is unidirectional too with the MSB transmitted first. SSI does not bolster spread postpone pay. Numerous encoder sellers make outright position encoders with SSI. The clock is high when latent. To start an information exchange, the clock goes low and the position is put away. On the primary rising edge of the clock flag, the MSB is moved out at the SSI encoder. On the second rising edge, the MSB-1 is moved out, etc, until the last piece (LSB) is moved out. After another clock cycle, the clock stays high until the following information exchange is begun. Contingent upon the time-out, the current locked position or another position esteem are transmitted on the following exchange. For points of interest, allude to the datasheet of the comparing SSI encoder.

THE MAIN FEATURES OF THIS DESIGN

• Universal equipment to interface to EnDat 2.2, BiSS, SSI, and HIPERFACE DSL encoders bolsters all relating standard information rates up to no less than 100-m link length
• Industry standard 24-V DC supply contribution with wide info voltage run from 15 to 60 V. The information is secured against invert extremity. Locally available DC/DC to created 3.3-V purpose of-load
• 3.3-V supply half-duplex RS-485 handset SN65HVD78 with 12-kV IEC-ESD and 4-kV EFT takes out cost for outer ESD segments.
• Encoder P/S with wide information extend (15 to 60 V) and programmable yield voltage 5.25 V or 11 V, consistent to EnDat 2.2, BiSS, or HIPERFACE DSL encoders
• OV, UV, and exact over current farthest point with short out security utilizing TI eFuse innovation with current screens (IMON) and blame Indicator. Choice to sidestep eFuse if insurance highlights not required
• Host processor interface (3.3-V I/O) to processors like Sitara AM437x or C2000 MCU to run the EnDat 2.2, BiSS, or HIPERFACE DSL ace.
• LEDs for status sign
• Meets EMC insusceptibility for ESD, EFT, surge, and directed RF with levels as indicated by IEC61800-3

HOST PROCESSOR INTERFACE

To change from one interface to alternate, this outline utilizes a simple MUX. The simple MUX is chosen rather than an immaculate advanced one on the grounds that the correspondence transport is bidirectional (the unadulterated computerized MUX is unidirectional). Moreover, to maintain a strategic distance from any effect on the correspondence between the host processor (ace) and the encoder, the spread postponement is a key parameter while selecting a legitimate MUX/DEMUX.

USE IN INDUSTRY

Rotating encoders are frequently used to track the position of the engine shaft on changeless magnet brushless engines, which are usually utilized on CNC machines, robots, and other mechanical hardware. Incremental (quadrature) encoders are utilized on acceptance engine sort servomotors, yet total encoders are utilized as a part of lasting magnet brushless engines, where appropriate. In these applications, the input gadget (encoder) assumes an imperative part in guaranteeing that the hardware works appropriately. The encoder synchronizes the relative rotor magnet and stator twisting positions to the current gave by the drive. Most extreme torque comes about if the current is connected to the windings when the rotor magnets are in a specific position extend with respect to the stator windings. The engine will perform inadequately or not under any condition if this planning is not balanced effectively. Inappropriate encoder arrangement on the engine can really make it run in reverse infrequently bringing about an unsafe flee condition. Rectify arrangement is fundamental to appropriate operation of these engines.

FAVORABLE CIRCUMSTANCES OF ABSOLUTE ENCODERS

A flat out encoder works as a non-unstable position check gadget. Genuine position is not lost if the power comes up short or the framework moves while power is off. A nonstop perusing of position is not required. This is especially valuable in applications, for example, satellite following radio wires, where infrequent position confirmation is all that is fundamental.

PROGRAMMING FLEXIBILITY

By taking out the requirement for framework homing, outright encoders can be controlled to give situating programs in light of building up reference from indicate point, as opposed to from a home position. Also, a chip interface module empowers the framework creator to program in a few working parameters, including determination. (See Serial-to-Parallel Converter Module). Wellbeing In a few applications, lost position could bring about harm to the apparatus or damage to the administrator. A flat out encoder gives position confirmation the minute power is up. Better Immunity to Electrical Noise Absolute encoders decide position by ceaselessly perusing a coded flag. Stray heartbeats, coming about because of electrical commotion, won't gather and precise position is accessible again on the following perusing Single Turn and Multi-Turn Absolute Encoders. As the name suggests, single turn encoders are most appropriate for short travel, movement control applications where position check is required inside a solitary turn of the encoder shaft. A multi-turn encoder is prescribed for applications including protracted or complex situating prerequisites.

POINTS OF INTEREST

- Excellent rakish precision

- Operating in extraordinary situations

- High unwavering quality

- Miniaturized encoders

- Large empty shaft encoders

- Very light weight

- Pancake encoders

- Cold excess on demand

- Easy adjustment to the application

CONCLUSION

There are many absolute position encoder standards that use RS-485 or RS-422 serial digital interfaces with, like EnDat2.2, BiSS, or HIPERFACEDSL. The design has been tested for EMC immunity against the electrostatic discharge (ESD), fast transient burst (EFT), surge, and conducted RF with levels specified per IEC61800-3. This design supports cable lengths of up to at least 100m. The connector in this design has dedicated pins for connecting a 2-wire HIPERFACEDSL encoder The absolute position encoder can be connected to the reference design either through a Sub D-15connector ora10-pin header. The signal from an absolute encoder gives an unambiguous position within the travel range without requiring knowledge of any previous position.

REFERENCES:

1. S.Zhan, M. H. Azarian and M. Pecht, "Reliability Issues of No-Clean Flux Technology with Lead-free Solder Alloy for High Density Printed Circuit Boards", 38th International Symposium on Microelectronics, pp.367–375, Philadelphia, PA, September 25–29, 2005.

2. V.Kavitha, V.Palanisamy, "New Burst Assembly and Scheduling T technique for Optical Burst Switching Networks", Journal of Computer Science, Vol. 9, Issue 8, pp.1030-1040, 2013.

3. Clyde F. Coombs Printed Circuits Handbook McGraw–Hill Professional, 2007 ISBN 0-07- 146734-3, pages 45–19

4. V.Kavitha, V.Palanisamy, "Simultaneous Multi-path Transmission for Burst Loss Recovery in Optical Burst Switching Networks", European Journal of Scientific Research, Vol. 87, Issue 3, pp.412-416, 2012.

5. Brunetti, Cledo (22 November 1948). New Advances in Printed Circuits. Washington DC: National Bureau of Standards.

6. K. Sundaravadivu and S. Bharathi, "STBC codes for generalized spatial modulation in MIMO systems," 2013 IEEE International Conference ON Emerging Trends in Computing, Communication and Nanotechnology (ICECCN), Tirunelveli, 2013, pp. 486-490. doi:10.1109/ICE-CCN.2013.6528548.

7. S.Palanivel Rajan, M.Paranthaman, Dr.C.Vivek, "Design and Enhancement of Wideband Reconfigurability using Two E-Shaped Patch Antenna", Asian Journal of Research in Social Sciences and Humanities, ISSN : 2249-7315, Vol.6, Issue 9, pp. 317-327, 2016.

8. C.Vivek, S.Palanivel Rajan, "Z-TCAM : An Efficient Memory Architecture Based TCAM", Asian Journal of Information Technology, Vol.15, Issue 3, pp.448-454, 2016.

9. S.Palanivel Rajan, K.Sheik Davood, "Performance Evaluation on Automatic Follicles Detection in the Ovary",

International Journal of Applied Engineering Research,Vol.10, Issue 55, pp.1-5, 2015.

10. Heath, Steve (2003). Embedded systems design. EDN series for design engineers (2 ed.). Newnes. p. 2. ISBN 978-0-7506-5546-0. An embedded system is a microprocessor based system that is built to control a function or a range of functions.

11. A.Manikandan, V.Nirmala, "A Low Cost Thermoelectric Refrigerator" in International Journal of Applied Engineering Research-IJAER, ISSN: 0973-4562, pp 3097-3100, 2015.

12. K. Kaarthik, P. Yuvarani, "Implementation of Distributed Operating System for industrial process automation using embedded technology", Journal of Chemical and Pharmaceutical Sciences, ISSN No.: 0974-2115, Special Issue 8, December 2016, pp. 99 - 103.

13. Michael Barr; Anthony J. Massa (2006). "Introduction". Programming embedded systems: with C and GNU development tools. O'Reilly. pp. 1–2. ISBN 978-0-596-00983-0.

14. A.Manikandan, J.Sakthivel, "IoT Based Real Time Traffic Analyzer" Journal of Chemical and Pharmaceutical Sciences, ISSN:0974-2115, pp 139-142, Dec 2016.

15. A.Manikandan, S.Ramalingam, V.Aathibhagavan, "Potholes Alert System for Riders", Advances in Natural and Applied Sciences, ISSN:1995-0772, pp 440-444, July 2016.