UNIT III

FREQUENCY RESPONSE OF AMPLIFIERS


Objectives:

• Discuss the frequency response of an amplifier
• Express the gain of an amplifier in decibels (dB)
• Analyze the low-frequency response of amplifiers
• Analyze the high-frequency response of amplifiers
• Analyze an amplifier for total frequency response
• Analyze multistage amplifiers for frequency response
• Measure the frequency response of an amplifier

3.1 Frequency Response
Basic Concept

\[ XC = \frac{1}{2\pi fc} \]

This formula shows that the capacitive reactance varies inversely with frequency. At lower frequencies the reactance is greater and it decreases as the frequency increases, at lower frequencies capacitively coupled amplifiers such as those in Fig3-1 have less voltage gain than they have at higher frequencies. The reason is that at lower frequencies more signal voltage is dropped across C1 and C3 because their reactances are higher. This higher signal voltage drop at lower frequencies reduces the voltage gain.
3.1.1 Effect of bypass capacitors

At lower frequencies, the reactance of the emitter bypasses capacitor, $C_2$ becomes significant and the emitter is at ac ground, the capacitive reactance $X_{C2}$ in parallel with $R_E$ creates an impedance that reduces the gain.

At higher frequencies, $X_C \approx 0 \Omega$ and the voltage gain is $A_v = \frac{R_C}{r_e}$

At lower frequencies, $X_C >> 0 \Omega$ and the voltage gain is $A_v = \frac{R_C}{(r_e + Z_e)}$

3.1.2 Effect of internal transistor capacitances

At high frequencies, the coupling and bypass capacitors become ac shorts and do not affect an amplifier's response. Internal transistor junction capacitances do come into play, reducing an amplifier's gain and introducing phase shift as the signal frequency increases. In BJT, $C_{be}$ ($C_{ib}$) is the B-E junction capacitance, and $C_{bc}$ ($C_{ob}$) is the B-C junction capacitance. In JFET, $C_{gs}$ ($C_{iss}$) is the G-S junction capacitance, and $C_{gd}$ ($C_{rss}$) is the G-D junction capacitance.
At lower frequencies, the internal capacitances have a very high reactance because of their low capacitance value (usually only a few pf) and the low frequency value. Therefore, they look like opens and have no effect on the transistor’s performance. As the frequency goes up, the internal capacitive reactance's go down, and at some point they begin to have a significant effect on the transistor's gain. When the reactance of Cbe (or Cgs) becomes small enough, a significant amount of the signal voltage is lost due to a voltage-divider effect of the source resistance and the reactance of Cbe Fig3-4(a). When the reactance of Cbc (or Cgd) becomes small enough, a significant amount of output signal voltage is fed back out of phase with the input (negative feedback), thus effectively reducing the voltage gain. Fig3-4(b)

**3.2 Miller’s Theorem**

Miller's theorem will be used later to simplify the analysis of inverting amplifiers at high frequencies where the internal transistor capacitances are important. The capacitance Cbc in BJTs between the input B and the output C is shown in Figure 3-5(a) in a generalized form. Av is the voltage gain of the amplifier at midrange frequencies, and C represents either Cbc.
Miller theorems state that \( C \) effectively appears as a capacitance from input to ground as shown in Fig 3-5(b) that can be expressed as follows:

\[
C_{\text{in}}(\text{Miller}) = C(\text{Av} + 1) \quad [3-1]
\]

This formula shows that \( C_{bc} \) has a much greater impact on input capacitance than its actual value. Fig 3-6 shows how this effective input capacitance appears in the actual equivalent circuit in parallel with \( C_{be} \).

Miller’s theorems also state that \( C \) effectively appears as a capacitance from output to ground as shown in Fig 3-5(b) that can be expressed as follows:

\[
C_{\text{out}}(\text{Miller}) = C\left(\frac{\text{Av} + 1}{\text{Av}}\right) \quad [3-2]
\]

This indicates that if the voltage gain is 10 or greater \( C_{\text{out}}(\text{Miller}) \) is approximately equal to \( C_{bc} \) because \((\text{Av} + 1) / \text{Av}\) is approximately equal to 1 Decibels.

Decibel is a form of gain measurement and is commonly used to express amplifier response. The decibel unit important in amplifier measurements, the basis for the decibel unit stems from the logarithmic response of the human ear to the intensity of sound. The decibel is a logarithm measurement of the ratio of one power to another or one voltage to another.

\[
\text{Ap(dB)} = 10 \log \text{Ap} \quad [3-3]
\]

\[
\text{Av(dB)} = 20 \log \text{Av} \quad [3-4]
\]

If \( \text{Av} \) is greater than 1, the dB gain is positive. If \( \text{Av} \) is less than 1, the dB gain is negative and is usually called attenuation.
**bel** (B) was defined by the following equation to relate power levels \( P_1 \) and \( P_2 \)

\[
G_{dB} = 10 \log_{10} \frac{P_2}{P_1}
\]

It was found that the bel was too large a unit of measurement for practical purposes, so the decibel (dB) was defined such that \( 10 \) decibels = 1 bel. Therefore,

\[
G_{dB} = 10 \log_{10} \frac{P_2}{P_1}
\]

**Note:**

Consider the following mathematical equations;

\[
a = b^x, \quad x = \log_b a
\]

\( a, b, \) and \( x \) are the same in each equation. If \( a \) determined by taking the same base \( b \) to the \( x \) power, the same \( x \) will result if the log of \( a \) is taken to the base \( b \). if \( b=10 \) and \( x=2 \),

\[
a = b^x = (10)^2 = 100
\]

\[
x = \log_{10} a = \log_{10} 100 = 2
\]

For the electrical/electronics, the base in the logarithmic equation is limited to 10

**Common logarithm:** \( x = \log_{10} a \)

For the neutral, the base in the logarithmic is limited to the number \( e=2.71828\ldots \)

**Natural logarithm:** \( y = \log_e a \)

The two are related by

\[
\log_e a = 2.3 \log_{10} a
\]

### 3.3 dB reference

It is often convenient in amplifiers to assign a certain value of gain as the 0 dB reference. This does not mean that the actual voltage gain is 1 (which is 0 dB); it means that the reference gain, is used as a reference with which to compare other values of gain and is therefore assigned a 0 dB value. The maximum gain is called the midrange gain and is assigned a 0 dB value. Any value of gain below midrange can be referenced to 0 dB and expressed as a negative dB value. For example, if the midrange voltage gain of a certain amplifier is 100 and the gain at a certain frequency below midrange is 50, then this reduced voltage gain can be expressed as: \( 20 \log (50/100) = 20 \log (0.5) = -6 \) dB. This indicates that it is 6 dB below the 0 dB reference. Halving the output voltage for a steady input voltage is always a 6 dB reduction in the gain. Correspondingly, a doubling of the output voltage is
always a 6 dB increase in the gain. Fig3-7 illustrates a normalized gain-versus frequency showing several dB points, the term normalized means that the midrange voltage gain is assigned a value of 1 or 0 dB.

![Normalized Av versus frequency curve](image)

Table 3-1 Decibel voltage values corresponding to doubling and halving of the voltage gain

<table>
<thead>
<tr>
<th>Voltage Gain (A&lt;sub&gt;v&lt;/sub&gt;)</th>
<th>dB (with respect to zero reference)</th>
</tr>
</thead>
<tbody>
<tr>
<td>32</td>
<td>20 log(32) = 30 dB</td>
</tr>
<tr>
<td>16</td>
<td>20 log(16) = 24 dB</td>
</tr>
<tr>
<td>8</td>
<td>20 log(8) = 18 dB</td>
</tr>
<tr>
<td>4</td>
<td>20 log(4) = 12 dB</td>
</tr>
<tr>
<td>2</td>
<td>20 log(2) = 6 dB</td>
</tr>
<tr>
<td>1</td>
<td>20 log(1) = 0 dB</td>
</tr>
<tr>
<td>0.707</td>
<td>20 log(0.707) = -3 dB</td>
</tr>
<tr>
<td>0.5</td>
<td>20 log(0.5) = -6 dB</td>
</tr>
<tr>
<td>0.25</td>
<td>20 log(0.25) = -12 dB</td>
</tr>
<tr>
<td>0.125</td>
<td>20 log(0.125) = -18 dB</td>
</tr>
<tr>
<td>0.0625</td>
<td>20 log(0.0625) = -24 dB</td>
</tr>
<tr>
<td>0.03125</td>
<td>20 log(0.03125) = -30 dB</td>
</tr>
</tbody>
</table>

### 3.4 The Critical Frequency

The critical frequency (cutoff frequency or corner frequency) is the frequency at which the output power drops to one-half of its midrange value; this corresponds to a 3dB reduction in the power gain, as expressed in dB by the following formula: \( \Delta p(dB) = 10 \log \left( \frac{0.5}{1} \right) = -3dB \). Also, at the critical frequency the output voltage is 0.707 percent of its midrange value and is expressed in dB as: \( \Delta v(dB) = 20 \log \left( \frac{0.707}{1} \right) = -3dB \).

At the critical frequency, the voltage gain is down 3 dB or is 70.7% of its midrange value. At this frequency, the power is one-half of its midrange value.

### 3.5 dB power Measurement

A unit that is often used in measuring power is the dBm, the term dBm means decibels referenced to 1 mW of power. When dBm is used, all power measurements are
relative to a reference level of 1 mW, a 3dBm increase corresponds to doubling of the power, and a 3 dBm decrease corresponds to a halving of the power. For example, +3 dBm corresponds to 2 mW (twice 1 mW), and -3 dBm corresponds to 0.5 mW (half of 1 mW).

<table>
<thead>
<tr>
<th>Power</th>
<th>dBm</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 mW</td>
<td>0 dBm</td>
</tr>
<tr>
<td>4 mW</td>
<td>3 dBm</td>
</tr>
<tr>
<td>8 mW</td>
<td>6 dBm</td>
</tr>
<tr>
<td>16 mW</td>
<td>9 dBm</td>
</tr>
<tr>
<td>32 mW</td>
<td>12 dBm</td>
</tr>
<tr>
<td>0.5 mW</td>
<td>-3 dBm</td>
</tr>
<tr>
<td>0.25 mW</td>
<td>-6 dBm</td>
</tr>
<tr>
<td>0.125 mW</td>
<td>-9 dBm</td>
</tr>
<tr>
<td>0.0625 mW</td>
<td>-12 dBm</td>
</tr>
<tr>
<td>0.03125 mW</td>
<td>-15 dBm</td>
</tr>
</tbody>
</table>

Table 3-2 power in terms of dBm

### 3.6 BJT Amplifier

A typical capacitively coupled CE Amp is shown in fig3-8. Assuming that the coupling and bypass capacitors are ideal shorts at the midrange signal frequency, you can determine the midrange voltage using Eq [3-5], where

\[
RC = RC || RL
\]

\[
Av(mid) = \frac{RC}{re}
\]  

[3-5]

Fig 3-8 a capacitive coupled amp

Fig 3-9 the low-frequency ac equivalent cct of amp

The BJT amplifier in Fig 3-8 has three high-pass RC circuits that affect its gain as the frequency is reduced below midrange. These are shown in the low-frequency ac equivalent circuit in Fig 3-9. Which represented midrange response (XC = 0Ω), the low-frequency equivalent circuit retains the coupling and bypass capacitors because XC is not small enough to neglect when the signal frequency is low. One RC circuit is formed by the input coupling capacitor Cl and the input resistance of the amplifier. The second RC circuit
is formed by the output coupling capacitor \( C_3 \), the resistance looking in at the collector, and the load resistance. The third RC circuit that affects the low frequency response is formed by the emitter-bypass capacitor \( C_2 \) and the resistance looking in at the emitter.

### 3.6.1 The input RC Circuit

The input RC circuit for the BJT amplifier in Fig3-8 is formed by \( C_1 \) and the amplifier’s input resistance is shown in Fig3-10, as the signal frequency decreases, \( X_{C1} \) increase, This causes less voltage across the input resistance of the amplifier at the base because more voltage is dropped across \( C_1 \) and because of this, the overall voltage gain of the amplifier is reduced.

The base voltage for the input RC circuit in Fig3-10 is:

\[
V_{\text{base}} = \left( \frac{R_{in}}{\sqrt{R_{in}^2 + X_{C1}^2}} \right) V_{in}
\]  

[3-6]

![Fig3-10 input RC circuit formed by C1 & Rin](image)

A critical point in the amplifier’s response occurs when the output voltage is 70.7 percent of its midrange value. This condition occurs in the input RC circuit when \( X_{C1} = R_{in} \)

\[
V_{\text{base}} = \left( \frac{R_{in}}{\sqrt{R_{in}^2 + R_{in}^2}} \right) V_{in} = \left( \frac{R_{in}}{\sqrt{2R_{in}^2}} \right) V_{in} = \left( \frac{1}{\sqrt{2}} \right) V_{in} = 0.707 V_{in}
\]  

[3-7]

In terms of measurement in decibels

\[
20 \log \left( \frac{V_{\text{base}}}{V_{in}} \right) = 20 \log (0.707) = -3 \text{ dB}
\]

### 3.6.1.1 Lower critical frequency

The condition where the gain is down 3 dB is logically called the -3dB point of the amplifier response; the overall gain is 3dB less than at midrange frequencies because of the attenuation of the input RC circuit. The frequency, \( f_c \) at which this condition occurs is called the lower critical frequency (lower cutoff frequency, lower corner frequency, or lower break frequency).
Example 1: for an input RC circuit in a certain Amp, \( R_{in} = 1 \, \text{k}\Omega \) & \( C_1 = 1 \, \mu\text{F} \). Neglect the source resistance (a) Determine the lower critical frequency (b) what is the attenuation of the RC circuit at the lower critical frequency (c) if the midrange voltage gain of the Amp is 100, what is the gain at the lower critical frequency?

Solution:

(a) \( f_c = \frac{1}{2\pi R_{in}C_1} = \frac{1}{2\pi(1.0 \, \text{k}\Omega)(1 \, \mu\text{F})} = 159 \, \text{Hz} \)

(b) At \( f_c \), \( X_{C1} = R_{in} \). Therefore,

\[ \text{Attenuation} = \frac{V_{base}}{V_{in}} = 0.707 \]

(c) \( A_v = 0.707 A_{v(mid)} = 0.707(100) = 70.7 \)

3.6.1.2 Voltage gain roll-off at low frequencies

The input RC circuit reduces the overall voltage gain of an amplifier by 3 dB when the frequency is reduced to the critical value \( f_C \). As the frequency continues to decrease below \( f_c \) the overall voltage gain also continues to decrease. The decrease in voltage gain with frequency is called roll-off. For each ten times reduction in frequency below \( f_C \) there is a 20 dB reduction in voltage gain. Let's take a frequency that is one-tenth of the critical frequency (\( f = 0.1f_C \)). Since \( X_{C1} = R_{in} \) at \( f_c \), then \( X_{C1} = 10R_{in} \) at 0.1fc because of the inverse relationship of \( X_{C1} \) and \( f \). the attenuation of the input RC circuit is, therefore,

\[
\text{Attenuation} = \frac{V_{base}}{V_{in}} = \frac{R_{in}}{\sqrt{R_{in}^2 + X_{C1}^2}} = \frac{R_{in}}{\sqrt{R_{in}^2 + (10R_{in})^2}} = \frac{R_{in}}{\sqrt{R_{in}^2 + 100R_{in}^2}} = \frac{R_{in}}{\sqrt{R_{in}(1 + 100)}} = \frac{R_{in}}{R_{in} \sqrt{101}} = \frac{1}{\sqrt{101}} \approx \frac{1}{10} = 0.1
\]
The dB attenuation is

\[ 20 \log \left( \frac{V_{\text{base}}}{V_{\text{in}}} \right) = 20 \log(0.1) = -20 \text{ dB} \]

### 3.6.1.3 dB/decade

A ten-time change in frequency is called a decade. So, for the input RC circuit, the attenuation is reduced by 20 dB for each decade that the frequency decreases below the critical frequency. This causes the overall voltage gain to drop 20 dB per decade. For example, if the frequency is reduced to one-hundredth of \( f_C \) (a two-decade decrease), the amplifier voltage gain drops 20 dB for each decade, giving a total decrease in voltage gain of \(-20 \text{ dB} + (-20 \text{ dB}) = -40 \text{ dB}\).

![dB Av versus f for the input RC circuit](image)

**Example 2:** the midrange voltage gain of a certain Amp is 100. the input RC cct has a lower critical frequency of 1kHz. Determine the actual voltage gain at \( f=1 \text{ kHz} \), \( f=100 \text{Hz} \), and \( f=10 \text{Hz} \).

**Solution:** when \( f = 1 \text{ kHz} \), \( A_v \) is 3dB less than at midrange. At -3dB, \( A_v \) reduced by 0.707

### 3.6.1.4 Phase shift in the input RC circuit

In addition to reducing the voltage gain, the input RC circuit also cause an increasing phase shift through an amplifier as the frequency decreases. At midrange frequencies the phase shift through the input RC circuit is approximately zero because \( XC_1 \approx 0 \Omega \), at lower frequencies, higher values of \( XC_1 \) cause a phase shift to be introduced, and the output voltage of the RC circuit leads the input voltage, the phase angle in an input RC circuit is expressed as:
\[ \theta = \tan^{-1}\left( \frac{Xc1}{Rin} \right) \]

At the critical frequency, \( XC1 = Rin \), so
\[ \theta = \tan^{-1}\left( \frac{0\Omega}{Rin} \right) = \tan^{-1}(0) = 0^\circ \]

A decade below the critical frequency, \( XC1 = 10 Rin \), so
\[ \theta = \tan^{-1}\left( \frac{10Rin}{Rin} \right) = \tan^{-1}(10) = 84.3^\circ \]

A continuation of this analysis will show that the phase shift through the input RC circuit approaches 90° as the frequency approaches zero. The result is that the voltage at the base of the transistor leads the input signal voltage in phase below midrange, as shown in fig3-13.

3.6.2 - The output RC circuit

The second high-pass RC circuit in the BJT amplifier is formed by the coupling capacitor \( C3 \), the resistance looking in at the collector, and the load resistance \( RL \). In determining the output resistance, looking in at the collector, the transistor is treated as an ideal current source and the upper end of RC is effectively at ac ground, as shown in fig 3-14(b)
Fig 3-14 Development of the equivalent low-frequency output RC circuit

Thevenizing the circuit to the left of capacitor C3 produces an equivalent voltage source equal to the collector voltage and a series resistance equal to RC, as shown in fig3-14(c).

\[ f_c = \frac{1}{2\pi(R_C + R_L)C_3} \]  

[3-9]

At the signal frequency decreases, \( X_C3 \) increases. This causes less voltage across the load resistance because more voltage is dropped across C3. The signal voltage is reduced by a factor of 0.707 when frequency is reduced to the lower critical value, \( f_C \), for the circuit. This corresponds to a 3 dB reduction in voltage gain.

**Example 3:** An output RC circuit in a certain amplifier, \( RC=10k\Omega, C_3=0.1\mu F, RL=10k\Omega \)

Determine the critical frequency (b) What is the attenuation of the output RC circuit at the critical frequency (c) if the midrange voltage gain of the amplifier is 50, what is the gain at the critical frequency?

**Solution:**

(a) \[ f_c = \frac{1}{2\pi(R_C + R_L)C_3} = \frac{1}{2\pi(20 k\Omega)(0.1 \mu F)} = 79.6 \text{ Hz} \]

(b) For the midrange frequencies, \( X_C3 \approx 0\Omega \), thus the attenuation of the circuit 

\[ \frac{V_{out}}{V_{collector}} = \frac{R_L}{R_C + R_L} = \frac{10 k\Omega}{20 k\Omega} = 0.5 \]
Or in dB, \( \frac{V_{out}}{V_{collector}} = 20 \log(0.5) = -6 \text{dB} \), this shows that, in this case, the midrange voltage gain is reduced by 6 dB because of the load resistor. At the critical frequency, \( XC_3 = RC + RL \) and the attenuation is

\[
\frac{V_{out}}{V_{in}} = \frac{R_L}{\sqrt{(RC + RL)^2 + X_{C3}^2}} = \frac{10 \text{ k\Omega}}{\sqrt{(20 \text{ k\Omega})^2 + (20 \text{ k\Omega})^2}} = 0.354
\]

Or in dB, \( \frac{V_{out}}{V_{collector}} = 20 \log(0.354) = -9 \text{dB} \). As you can see, the gain at \( fc \) is 3dB less than the gain at midrange

\[
(c) \quad A_v = 0.707 A_v(mid) = 0.707(50) = 35.4
\]

3.6.2.1 Phase shift in the output RC circuit

The phase shift in the output RC circuit is

\[
\theta = \tan^{-1}\left(\frac{X_{C3}}{RC + RL}\right)
\]

\( \theta \approx 0 \) for the midrange frequency and approaches 90° as the frequency approaches zero (\( XC_3 \) approaches infinity). At the critical frequency \( f_C \), the phase shift is 45°.

3.6.3 The bypass RC circuit

The third RC circuit that affects the low-frequency gain of the BJT amplifier is the bypass capacitor \( C_2 \). For midrange frequencies, it is assumed that \( XC_2 \approx 0 \Omega \), effectively shorting the emitter to ground so that the amplifier gain is: \( Av = \frac{RC}{re} \)

![Fig 3-15 at low frequencies \( XC_2 \parallel RE \) reduces \( Av \)]

As the frequency is reduced, \( XC_2 \) increases and provides a sufficiently low reactance to effectively place the emitter at ac ground. Because the impedance from emitter to ground increases, the gain decreases is: \( Av = \frac{RC}{(re + Re)} \).
Re is replaced by an impedance formed by RE in parallel with XC, The bypass RC circuit is formed by C2 and the resistance looking in at emitter Rin(emitter), Fig3-16(a). First, Thevenin's theorem is applied looking from the base of the transistor toward the input source Vin Fig3-16(b). This results in an equivalent resistance (Rth) and an equivalent voltage source Vth(1) in series with the base, Fig3-16(c). The resistance looking in at the emitter is determined with the equivalent input source shorted, Fig3-16(d),

\[
R_{\text{in(emitter)}} = \frac{V_e}{I_v} + r_e' \equiv \frac{V_b}{\beta_{ac} I_b} + r_e' = \frac{I_b R_{th}}{\beta_{ac} I_b} + r_e'
\]

Looking from capacitor C2, Rth / βac + re is in parallel with RE, Fig3-16(e), thevenizing again, we get the equivalent RC circuit Fig3-16(f), the fc for this equivalent bypass RC circuit is

\[
f_c = \frac{1}{2\pi \left[ (r_e' + R_{th}/\beta_{ac}) || R_E \right] C_2}
\]
**Example 4**: Determine $f_c$ of the bypass RC circuit for the amplifier in fig3-17 ($r_e = 12 \Omega$)

![Circuit Diagram]

**Solution**: Thevenize the base circuit (looking from the base toward the input source)

$$R_{in} = R_1 || R_2 || R_3 = 62 \, k\Omega || 22 \, k\Omega || 1.0 \, k\Omega = 942 \, \Omega$$

$$R_{in(\text{emitter})} = r_e' + \frac{R_{th}}{\beta_{ac}} = 12 \, \Omega + 9.42 \, \Omega = 21.4 \, \Omega$$

$$R_{in(\text{emitter})} || R_E = 21.4 \, \Omega || 1000 \, \Omega = 21 \, \Omega$$

$$f_c = \frac{1}{2\pi(R_{in(\text{emitter})} || R_E)C_2} = \frac{1}{2\pi(21 \, \Omega)(100 \, \mu\text{F})} = 75.8 \, \text{Hz}$$

**3.7 The Bode Plot**

A plot of dB voltage gain versus frequency on semilog graph paper (logarithmic horizontal axis scale and a linear vertical axis scale) is called a bode plot. The source of the spacing between the lines of the log plot is shown on fig3-18, the log of 2 to the base 10 is approximately 0.3. The distance from 1 (log 10 1 = 0) to 2 is therefore 30% of the span.

![Semi log graph paper]
It is important to note the resulting numerical value and the spacing since plots will typically only have the tic marks indicated in Fig 3-19 due to a lack of space.

Fig 3-19 identifying the numerical values of the marks on the log scale

### 3.7.1 Total Low-Frequency Response of an Amplifier

The critical frequencies of the three RC circuits are not necessarily all equal. If one of the RC circuits has a critical (break) frequency higher than the other two, then it is dominant RC circuit. The dominant circuit determines the frequency at which the overall voltage gain of the amplifier begins to drop at -20 dB/decade roll-off below their respective critical (break) frequencies. In fig 3-21 each RC circuit has a different critical frequency, the input RC circuit is dominant (highest fc) in this case and the bypass RC has the lowest.

As the frequency is reduced from midrange, the first "break point" occurs at the critical frequency of the input RC circuit, fc(input), and the gain begins to drop at -20dB/decade. This constant roll-off rate continues until the critical frequency of the output RC circuit, fc(output), is reached. At this break point, the output RC circuit adds another -20 dB/decade to make a total roll-off of -40 dB/decade. This constant -40 dB/decade roll-off continues until the critical frequency of the bypass RC circuit, fc(bypass), is reached. At this break point, the bypass RC circuit adds still another -20dB/decade, making the gain roll-off at -60 dB/decade.

Fig 3-21 Bode plot of a BJT amp response for three low-frequency RC circuits
If all RC circuits have the same critical frequency, the response curve has one break point at that value of \( f_c \), and the voltage gain rolls off at -60 dB/decade below that value, as shown by Fig 3-22. Actually, the midrange voltage gain does not extend down to the dominant critical frequency but is really at -9 dB below the midrange voltage gain at that (-3 dB for each RC circuit).

**Fig 3-22** Composite Bode plot of an amplifier response where all RC circuits have the same \( f_c \).

### 3.8 High-Frequency Amplifier Response

A high frequency ac equivalent circuit for the BJT amplifier in Fig 3-25(a) is shown in Fig 3-25(b). The internal capacitances, \( C_{be} \) and \( C_{bc} \), which are significant only at high frequencies, do appear in the diagram.

**Fig 3-25** capacitively coupled amplifier and its high-frequency equivalent circuit

#### 3.8.1 Miller’s Theorem in high-frequency analysis

By applying Miller’s theorem to the circuit in Fig 3-25(b) and using the midrange voltage gain, you have a circuit that can be analyzed for high-frequency response.
\[ C_{\text{in(miller)}} = C_{bc}(A_v + 1) \]  
\[ C_{\text{out(miller)}} = C_{bc}\left(\frac{A_v + 1}{A_v}\right) \]

Cbe simply appears as a capacitance to ac ground, in parallel with Cin(Miller).

These two capacitances create a high-frequency input RC circuit and a high-frequency output RC circuit. These two circuits differ from the low-frequency input and output circuit, which act as high-pass filters, because the capacitances go to ground and therefore act as low-pass filters.

3.8.2 The Input RC Circuit

At high frequencies, the input circuit is as shown in Fig3-27(a), where \( \beta_{ac_re} \) is the input resistance at the base of the transistor because the bypass capacitor effectively shorts the emitter to ground. By combining Cbe and Cin(Miller) in parallel and repositioning, you get the simplified circuit shown in Fig3-27(b). Next, by thevenizing the circuit to the left of the capacitor, the input RC circuit is reduced to the equivalent form shown in Fig3-27(c).

As the frequency increases, the capacitive reactance becomes smaller. This cause the signal voltage at the base to decrease, so the amplifier’s voltage gain decreases. The reason for this is that the capacitance and resistance act as a voltage divider and, as the frequency increases, more voltage is dropped across the resistance and less across the capacitance.

At the critical frequency, the gain is 3 dB less than its midrange value. Just as with the low-frequency response, the critical high frequency, \( f_c \), is the frequency at which the capacitive reactance is equal to the total resistance

\[
X_{C_{tot}} = R_s \parallel R_1 \parallel R_2 \parallel \beta_{ac} r_e'
\]

\[
\frac{1}{2\pi f_c C_{tot}} = R_s \parallel R_1 \parallel R_2 \parallel \beta_{ac} r_e'
\]
Fig 3-27 Development of the equivalent high-frequency input RC circuit

\[
f_c = \frac{1}{2\pi(R_s \parallel R_1 \parallel R_2 \parallel \beta_{ac} r'_e) C_{tot}}
\]

Where \( R_s \) is the resistance of the signal source and \( C_{tot} = C_{be} + C_{in(Miller)} \)
As the frequency goes above in the input RC circuit causes the gain to roll off at a rate of -20 dB/decade just as with the low-frequency response.

**Example 6**: Derive the input RC circuit for the BJT amplifier in fig 3-28, also determine the critical frequency. The transistor’s data sheet provides the following: \( \beta_{as} = 125 \), \( C_{be} = 20 \) pF, and \( C_{bc} = 2.4 \) pF

**Solution**: First, find \( r_e \) as follows:
Next, in order to determine the capacitance, you must calculate the midrange gain of the amplifier so that you can apply Miller’s theorem.

\[ A_{V(mid)} = \frac{R_c}{r'_e} = \frac{R_c}{r'_e} = \frac{1.1 \text{k}\Omega}{11.1 \text{\Omega}} = 99 \]

Apply Miller’s theorem.

\[ C_{in(Miller)} = C_{be}(A_{V(mid)} + 1) = (2.4 \text{pF})(100) = 240 \text{pF} \]

The total input capacitance is \( C_{in(Miller)} \) in parallel with \( C_{be} \).

\[ C_{in(total)} = C_{in(Miller)} + C_{be} = 240 \text{pF} + 20 \text{pF} = 260 \text{pF} \]

The resulting high-frequency input RC circuit is shown in fig 3-29. The critical frequency is

\[ f_c = \frac{1}{2\pi(R_{in(total)}(C_{M(total)})} = \frac{1}{2\pi(378 \text{\Omega})(260 \text{pF})} = 1.62 \text{MHz} \]
3.8.2.1 Phase shift of the input RC circuit

Because the output voltage of a high-frequency input RC circuit is across the capacitor, the output of the circuit lags the input. The phase angle is expressed as

$$\theta = \tan^{-1}\left(\frac{R_s \parallel R_1 \parallel R_2 \parallel \beta_{ac} r_v'}{X_{C_{in}}}\right)$$

At the critical frequency, the phase angle is 45° with the signal voltage at the base of the transistor lagging the input signal. As the frequency increases above $f_c$, the phase angle increases above 45° and approaches 90° when the frequency is sufficiently high.

3.8.3 The output RC circuit

The high-frequency output RC circuit is formed by the Miller output capacitance and the resistance looking in at the collector, as shown in fig3-30(a). In determining the output resistance, the transistor is treated as a current source (open) and one end of RC is effectively ac ground, as shown in Fig3-30(b). By rearranging the position of the capacitance in the diagram and thevenizing the circuit to the left, as shown in Fig3-30(c), you get the equivalent circuit in fig3-30(d). The equivalent output RC circuit consists of a resistance equal to RC and RL in parallel in series with a capacitance which is determined by the following miller’s formula:

$$C_{\text{out(Miller)}} = C_{bc}\left(\frac{A_v + 1}{A_v}\right)$$

If the voltage gain is at least 10, this formula can be approximated as

$$C_{\text{out(Miller)}} \cong C_{bc}$$

The critical frequency is determine with the following equation, where $RC=RC\parallel RL$

$$f_c = \frac{1}{2\pi R_c C_{\text{out(Miller)}}}$$

The output RC circuit reduces the gain by 3 dB at the critical frequency. When the frequency goes above the critical value, the gain drops at a -20dB/decade rate. The phase shift introduced by the output RC circuit is:

$$\theta = \tan^{-1}\left(\frac{R_c}{X_{C_{out(Miller)}}}\right)$$

[3-15]
Example 7: Determine the critical frequency of the amplifier in Example 6 (fig 3-28) due to its output RC circuit.

Solution: The Miller output capacitance is calculated as follows:

$$C_{out(Miller)} = C_{bc} \left( \frac{A_v + 1}{A_v} \right) = (2.4 \text{ pF}) \left( \frac{99 + 1}{99} \right) \approx 2.4 \text{ pF}$$

The equivalent resistance is:

$$R_c = R_C \parallel R_f = 2.2 \text{ k}\Omega \parallel 2.2 \text{ k}\Omega = 1.1 \text{ k}\Omega$$

The equivalent output RC circuit is shown in fig3-31, and the $f_c$ is determined as follows:

$$f_c = \frac{1}{2\pi R_c C_{bc}} \approx \frac{1}{2\pi (1.1 \text{ k}\Omega)(2.4 \text{ pF})} = 60.3 \text{ MHz}$$
3.8.4 Total High-Frequency Response of an Amplifier

The two RC circuits created by the internal transistor capacitances influence the high frequency response of BJT amplifiers. As the frequency increases and reaches the high end of its midrange values, one of the RC will cause the amplifier’s gain to begin dropping off. The frequency at which this occurs is the dominant critical frequency; it is the lower of the two critical high frequencies. An ideal high-frequency Bode plot is shown in Fig 3-32(a). It shows the first break point at \( fc(\text{input}) \) where the voltage gain begins to roll off at \(-20\text{dB/decade}\). At \( fc(\text{output}) \), the gain begins dropping at \(-40\text{dB/decade}\) because each RC circuit is providing a \(-20\text{dB/decade}\) roll-off, Fig 3-32(b) shows a non ideal Bode plot where the voltage gain is actually \(-3\text{dB}\) below midrange at \( fc(\text{input}) \).

![Fig 3-32 High Frequency Bode plots](image)

3.9 Total Amplifier Frequency Response

Fig 3-33(b) shows a generalized ideal response curve (Bode plot) for the BJT Amplifier shown in Fig 3-33(a). The three break points at the lower frequencies (\( fc_1 \), \( fc_2 \), and \( fc_3 \)) are produced by the three low-frequency RC circuit formed by the coupling and bypass capacitors. The break points at the upper critical frequencies, \( fc_4 \) and \( fc_5 \), are produced by the two high frequency RC circuits formed by the transistor’s internal capacitances. The two dominant critical frequencies, \( fc_3 \) and \( fc_4 \) (fig 3-33(b)), these two frequencies are where the voltage gain of the amplifier is \(3\text{dB}\) below its midrange value. These dominant frequencies are referred to as the lower critical frequency, \( fc_L \), and the upper critical frequency, \( fc_u \).

![a BJT amplifier and its generalized ideal response curve (Bode plot)](image)
**3.10 Band width**

An amplifier normally operates with signal frequencies between \( f_{CL} \) and \( f_{CU} \). If the signal frequency drops below \( f_{CL} \), the gain and thus the output signal level drops at 20 dB/decade until the next critical frequency is reached. The same occurs when the signal frequency goes above \( f_{CU} \). The range (band) of frequencies lying between \( f_{CL} \) and \( f_{CU} \) is defined as the bandwidth of the amplifier. Only the dominant critical frequencies appear in the response curve because they determine the bandwidth. The amplifier’s bandwidth is expressed in units of hertz as

\[
BW = f_{CU} - f_{CL}
\]

Ideally, all signal frequencies lying in an amplifier’s bandwidth are amplified equally. For example: if a 10 mV rms signal is applied to an amplifier with a voltage gain of 20, it is amplified to 200 mV rms for all frequencies in the bandwidth. Actually, the gain is down 3 dB at \( f_{CL} \) and \( f_{CU} \).

**Example 8:** What is the bandwidth of an amplifier having an \( f_{CL} \) of 200 Hz and \( f_{CU} \) of 2 KHz?

**Solution**

\[
BW = f_{CU} - f_{CL} = 2000 \text{ Hz} - 200 \text{ Hz} = 1800 \text{ Hz}
\]

If \( f_{CL} \) is increased, does the bandwidth increase or decrease? If \( f_{CU} \) is increased, does the bandwidth increase or decrease?

**3.11 Gain-Bandwidth Product**

One characteristic of amplifiers is that the product of the voltage gain and the bandwidth is always constant when the roll-off is -20dB/decade. This characteristic is called the gain bandwidth product. Let’s assume that the lower critical frequency of a particular amplifier is much less than the upper critical frequency.
3.12 Unity-Gain Frequency

The simplified Bode plot for this condition is shown in Fig 3-35. Notice that \( f_{cl} \) is neglected because it is so much smaller than \( f_{cu} \) and the bandwidth approximately equals \( f_{cu} \). Beginning at \( f_{cu} \), the gain rolls off until unity gain (0 dB) is reached. The frequency at which the amplifier’s gain is 1 is called the unity-gain frequency, \( f_T \).

\[
\frac{f_{cl}}{f_{cu}} \ll 1
\]

\[
BW = f_{cu} - f_{cl} \approx f_{cu}
\]

Example 9: A certain transistor has an \( f_T \) of 175 MHz. When this transistor is used in an amplifier with a midrange voltage gain of 50, what bandwidth can be achieved ideally?

Solution:

\[
f_T = A_{v(mid)}BW
\]

\[
BW = \frac{f_T}{A_{v(mid)}} = \frac{175 \text{ MHz}}{50} = 3.5 \text{ MHz}
\]

3.13 Half-Power Point

The upper and lower critical frequencies are sometimes called the half-power frequencies, this term is derived from the fact that the output power of an amplifier at its critical frequencies is one-half of its midrange power, as previously mentioned. This can be
shown of follows, starting with the fact that the output voltage is 0.707 of its midrange value at the critical frequencies
\[ V_{\text{out}(f_c)} = 0.707 V_{\text{out(mid)}} \]
\[ P_{\text{out}(f_c)} = \frac{V_{\text{out}(f_c)}^2}{R_{\text{out}}} = \frac{(0.707 V_{\text{out(mid)}})^2}{R_{\text{out}}} = \frac{0.5 V_{\text{out(mid)}}^2}{R_{\text{out}}} = 0.5 P_{\text{out(mid)}} \]

3.14 Multistage Amplifier

One of the advantages of the logarithmic relationship is the manner in which it can be applied to cascaded stages, for example, the magnitude of the overall voltage gain of a cascaded system is given by:

\[ |A_{v_{\text{in}}}| = |A_{v_1}| |A_{v_2}| |A_{v_3}| \cdots |A_{v_n}| \]

Applying the proper logarithmic relationship results in:

\[ G_v = 20 \log_{10} |A_{v_1}| = 20 \log_{10} |A_{v_2}| + 20 \log_{10} |A_{v_3}| \cdots + 20 \log_{10} |A_{v_n}| \quad \text{(dB)} \]

i.e. the gain of a cascaded system is simply the sum of the decibel gains of each stage

\[ G_{\text{dB}_1} = G_{\text{dB}_2} + G_{\text{dB}_3} + \cdots + G_{\text{dB}_n} \quad \text{dB} \]

3.14.1 Methods of Coupling Transistor

The circuitry used to connect the output of one stage of a multistage amplifier to the input of the next stage is called the coupling method, one such method:

3.14.1.1 Cascade Amplifier

A cascade connection is a series connection it has one on top of another, for a cascade connection, amplification is the product of the stage gains, a cascade connection provides a high input impedance with low voltage gain to ensure that the Miller capacitance is at a minimum with the CB stage providing good high-frequency operation and a low output impedance.

![Fig 3-36 Cascade configuration](image)
When amplifier stages are cascaded to form a multistage amplifier, the dominant frequency response is determined by the responses of the individual stages. There are two cases to consider:

1. Each stage has a different lower critical frequency and a different upper critical frequency
2. Each stage has the same lower critical frequency and the same upper critical frequency

**1-Different Critical Frequencies**

When the lower critical frequency, \( f_{CL} \), of each amplifier stage is different, the dominant lower critical frequency, \( f'_{CL} \), equals the critical frequency of the stage with the highest \( f_{CL} \). When the upper critical frequency \( f_{CU} \), of each amplifier stage is different, the dominant upper critical frequency \( f'_{CU} \), equals the critical frequency of the stage with the lowest \( f_{CU} \).

**Overall Bandwidth**

The bandwidth of a multistage amplifier is the difference between the dominant lower critical frequency and the dominant upper critical frequency.

\[
BW = f'_{CU} - f'_{CL}
\]

**Example 3**: In a certain 2-stage amplifier, one stage has a lower critical frequency of 850 Hz and an upper critical frequency of 100 kHz. The other has a lower critical frequency of 1 kHz and an upper critical frequency of 230 kHz. Determine the overall bandwidth of the 2-stage amplifier.

**Solution**:

\[
\begin{align*}
    f'_{CL} &= 1 \text{ kHz} \\
    f'_{CU} &= 100 \text{ kHz} \\
    BW &= f'_{CU} - f'_{CL} = 100 \text{ kHz} - 1 \text{ kHz} = 99 \text{ kHz}
\end{align*}
\]

**2-Equal Critical Frequencies**

When each amplifier stage in a multi-stage arrangement has equal critical frequencies, the dominant lower critical frequency is increased by a factor of \( \frac{1}{\sqrt{2^{1/n} - 1}} \) as shown by the following formula (\( n \) is the number of stages in the multi-stage amplifier):

\[
f'_{CL} = \frac{f_{CL}}{\sqrt{2^{1/n} - 1}} \tag{3-18}
\]

When the upper critical frequencies of each stage are all the same, the dominant upper critical frequency is reduced by a factor of \( \sqrt{2^{1/n} - 1} \), as shown by the following formula:

\[
f'_{CU} = f_{CU} \sqrt{2^{1/n} - 1} \tag{3-19}
\]

**Example 11**: Both stages in a certain 2-stage amplifier have a lower critical frequency of 500Hz and an upper critical frequency of 80 kHz. Determine the overall bandwidth.
Example 12: Calculate the voltage gain for the cascade amplifier of fig 3-37

Solution:

\[ f'_{cl} = \frac{f_{cl}}{\sqrt{2^1/n - 1}} = \frac{500 \text{ Hz}}{\sqrt{2^{0.5} - 1}} = \frac{500 \text{ Hz}}{0.644} = 776 \text{ Hz} \]

\[ f'_{cu} = f_{cu} \sqrt{2^{1/n} - 1} = (80 \text{ kHz})(0.644) = 51.5 \text{ kHz} \]

\[ \text{BW} = f'_{cu} - f'_{cl} = 51.5 \text{ kHz} - 776 \text{ Hz} = 50.7 \text{ kHz} \]

\[ V_{B_1} = 4.9 \text{ V}, \quad V_{B_2} = 10.8 \text{ V}, \quad I_{C_1} \approx I_{C_2} = 3.8 \text{ mA} \]

\[ r_e = \frac{26}{3.8} = 6.8 \Omega \]

\[ A_v = \frac{R_C}{r_e} = \frac{26}{6.8} = -1 \]

\[ A_{v_2} = \frac{R_C}{r_e} = \frac{1.8 \text{ k}\Omega}{6.8 \Omega} = 265 \]

\[ A_v = A_{v_1}A_{v_2} = (-1)(265) = -265 \]
3.14.1.2-Capacitor coupling (RC coupling)

Capacitor coupling, also called RC Coupling because the inter stage circuitry is equivalent to a high-pass RC network. RC coupling is used to prevent dc current from flowing between the output of one amplifier stage and the input of the next stage. The capacitor connected in the path between amplifier stages makes it possible to have a dc bias voltage at the output of one stage that is different from the dc bias voltage at the input to the next stage. This idea is illustrated in Fig3-38.

![Fig3-38](image)

**Example 13:** Fig3-39 shows an amplifier consisting of a CE stage driving an E-follower stage; the transistors have the following parameter values:

![Fig3-39 network for Ex 13](image)

- \( Q_1: r_e = 15 \, \Omega, \, \beta_1 = 180, \, r_e \approx \infty \)
- \( Q_2: r_e = 25 \, \Omega, \, \beta_2 = 100 \)
Solution:

\[ f_1(C_1) = \frac{1}{2\pi \left( r_{in}(\text{stage 1}) + r_2 \right) C_1} = \frac{1}{2\pi (2.48 \times 10^4 + 100) \times 10^{-6}} = 10.3 \text{ Hz} \]

\[ f_1(C_2) = \frac{1}{2\pi R_e C_F} \]

where \( C_E = C_2 = 40 \, \mu F \) and

\[ R_e = \frac{R_E \left( \frac{r_s \| r_g}{\beta_1} + r_e \right)}{\left( 1.5 \times 10^3 \right) \left( \frac{100 \| (150 \times 10^3) \| (39 \times 10^3)}{180} + 15 \right)} = 15 \, \Omega \]

\[ f_1(C_2) = \frac{1}{2\pi (15) (40 \times 10^{-6})} = 265.3 \text{ Hz} \]

\[ f_1(C_3) = \frac{1}{2\pi \left( r_{in}(\text{stage 1}) + r_{in}(\text{stage 2}) \right) C_3} \]

\[ = \frac{1}{2\pi (4.7 \times 10^3 + 5.9 \times 10^3)(9.4 \times 10^{-6})} = 37.5 \text{ Hz} \]

\[ f_1(C_4) = \frac{1}{2\pi \left( r_{in}(\text{stage 2}) + R_L \right) C_4} = \frac{1}{2\pi (64.8 + 50) (20 \times 10^{-6})} = 69.3 \text{ Hz} \]

Fig 3-41 Bode plot for the gain
\( C_1 = \text{Cout(\text{stage 1}) + Cin(\text{stage 2})} \)
3.14.1.3 Direct-Coupled Amplifier

Direct coupling is the coupling method in which the output of one stage is electrically connected directly to the input of the next stage. In other words, both the dc and ac voltages at the output of one stage are identical to those at the input of the next stage. Clearly, any change in the dc voltage at the output of one stage produces an identical change in dc voltage at the input to the next stage, so a direct-coupled amplifier behaves like a direct-current amplifier. Direct coupling is used in differential and operational amplifiers.

The output of the first stage (collector of Q₁) is connected directly to the input of the second stage (base of Q₂) we will first analyze the dc bias of the circuit and then consider its ac performance. The current in \(RC₁ = IC₁ + IB₂\)

\(IB₂\) is negligibly small in comparison to \(IC₁\), \(VB₁\) is determined essentially by the \(R₁-R₂\) voltage divider

\[
V_{E₁} = V_{B₁} - 0.7
\]

\[
V_{C₁} = V_{CC} - I_{C₁}R_{C₁}
\]

\[
V_{CE₁} = V_{C₁} - V_{E₁}
\]

\[
V_{E₂} = V_{C₁} - 0.7
\]

\[
V_{C₂} = V_{CC} - I_{C₂}R_{C₂}
\]

\[
V_{CE₂} = V_{C₂} - V_{E₂}
\]

The important point to note is that \(VC₁ = VB₂\). The voltage gain of the first stage is

\[
A_{v₁} ≈ \frac{-r_{o}(stage \ 1) \ || \ r_{in}(stage \ 2)}{r_{e₁} + R_{E₁}}
\]
Finally, the overall gain is the product of the stage gains:

$$A_v(overall) = A_{v1}A_{v2}$$

If a load resistance $R_L$ is direct-coupled between the output (collector of $Q_2$) and ground, then the ac load resistance on the second stage is $r_L = \frac{R_{C2}}{R_L}$

It is important to realize that direct-coupling an output load resistance changes the dc value of $V_{C2}$ and $V_{CE2}$, to demonstrate this fact, let us regard the transistor as a constant-current source, as shown in fig3-43(b). We can then apply $V_L (= V_C)$ due to each source in the circuit, as shown in fig3-43(c) and (d).

![Fig3-43 computing the dc voltage across a direct-connected load $R_L$.](image)

$$V_L = \left( \frac{R_L}{R_C + R_L} \right) V_{CC} - I_C \left( \frac{R_C}{R_L + R_C} \right) R_L = \left( \frac{R_L}{R_L + R_C} \right) (V_{CC} - I_C R_C)$$

Combining the contributions of each source leads to:

$$V_L = V_C = \left( \frac{R_L}{R_L + R_C} \right) (V_{CC} - I_C R_C)$$
Questions for review
1- In an ac amplifier, which capacitors affect the low frequency gain?
2- How is the high frequency gain of an amplifier limited?
3- When can coupling and bypass capacitors be neglected?
4- Determine Cin(Miller) if Av = 50 and Cbc = 5pF?
5- Determine Cout(Miller) if Av = 25 and Cbc = 3 pF?
6- How much increase in actual voltage gain corresponds to +12 dB?
7- Convert a power gain of 25 to decibels
8- What power corresponds to 0 dBm?
9- A certain BJT amplifier exhibits three critical frequencies in its low-frequency response: fc1 = 130Hz, fc2 = 167 Hz, fc3 = 75 Hz. Which is the dominant critical frequency?
10- If the midrange voltage gain of the amplifier in Q:9 is 50 dB, what is the gain at the dominant fc?
11- A certain RC circuit has an fc = 235 Hz, above which the attenuation is 0 dB. What is the dB attenuation at 23.5 Hz?
12- What is the amount of phase shift contributed by an input circuit when XC = 0.5 Rin at a certain frequency below fc1?
13- What determines the high-frequency response of an amplifier?
14- If an amplifier has a midrange voltage gain of 80, the transistor’s Cbc is 4 pF, and Cbe = 8 pF, what is the total input capacitance?
15- A certain amplifier has fc(input) = 3.5 MHz and fc(output) = 8.2 MHz. Which circuit dominates the high-frequency response?
16- What is the voltage gain of an amplifier at fT?
17- What is the bandwidth of an amplifier when fcu = 25 kHz and fcL = 100Hz?
18- The fT of a certain transistor is 130 MHz. What voltage gain can be achieved with a bandwidth of 50 MHz?
19- One stage in an amplifier has fcL = 1 kHz and the other stage has fcL = 325 Hz. What is the dominant lower critical frequency?
20- In a certain 3-stage amplifier fcu(1) = 50 kHz, fcu(2) = 55 kHz, and fcu(3) = 49 kHz. What is the dominant upper frequency?
21- When more identical stages are added to a multistage amplifier with each stage having the same critical frequency, does the bandwidth increase or decrease?
22- The logarithm of a number will give you the power to which the base must be brought to obtain the same number. If the base is 10, it is referred to as the common logarithm; if the base is e = 2.71828…, it is called the natural logarithm.
23- Since the decibel rating of any piece of equipment is a comparison between levels, a reference level must be selected for each area of application. For audio system, terms the reference level is generally accepted as 1 mW.
24- The dB gain of cascaded systems is simply the sum of the dB gains of each stage.
25- It is the capacitive elements of a network that determine the bandwidth of a system. The larger capacitive elements of the basic design will determine the low cutoff frequency, whereas the smaller parasitic capacitors will determine the high cutoff frequencies.
5- The frequencies at which the gain drops to 70.7% of the mid-band value are called the cutoff, corner, band, break, or half-power frequencies.
26-The **narrower** the bandwidth, the **smaller** the range of frequencies that will permit a transfer of power to the load that is at least 50% of the mid-band level.

27-A change in frequency by a factor of 2, equivalent to 1 decade, results in a 6-dB change in **gain**. For a 10:1 change in frequency, there is a **20-dB change in gain**.

28-For any **inverting** amplifier, the input capacitance will be increased by a miller **effect** capacitance determined by the **gain** of the amplifier and the **interelectrode** (parasitic) capacitance between the input and output terminals of the active device.